REMARKS

i. INTERVIEW SUMMARY UNDER 37 C.F.R. §1.133 AND MPEP §713.04

A telephonic interview in the above-referenced case was conducted on May 2, 2005, with Examiner Nguyen and Trueman H. Denny III. The Office Action mailed on **February 9, 2005** was discussed. Specifically, the rejections **Claims 10 and 11** which. In considering the proposed claims (now being presented) the Examiner indicated that the rejection under **35 U.S.C. §112** second paragraph would be overcome by amending **Claim 10** to recite *"electrical communication"* between the elements. Additionally the Examiner indicated that the **35 U.S.C. §102(b)** rejection of **Claim 10** may be overcome by distinguishing the "*non-volatile two-terminal cross point memory array*" of the present application over the volatile DRAM array of *Iwata*. The Applicants wish to sincerely thank the Examiner for his time and attention in this case.

Applicant thanks the Examiner for the thoughtful review of the application. The Applicant notes with appreciation that **Claims 1 – 9** and **12 – 26** have been allowed by the Examiner. The status of the claims is as follows: **Claims 1 – 26** are pending; **Claims 11** and **10** stand rejected under second paragraph of **35 U.S.C. §112** and under **35 U.S.C. §102(b)** in view of U.S. Patent **6,778,424** to *Iwata* et al; and **Claims 10** and **11** have been amended herein to overcome the aforementioned rejections.

II. ARGUMENT

a. Rejection of Claims 11 & 10 under second paragraph of 35 U.S.C. §112

Independent **Claim 10** has been amended herein to particularly point out and distinctly claim the subject matter the Applicant regards as his invention. Specifically, **Claim 10** was amended to replace "*electrically connected*" and "*the electrical connections*" with "electrical communication" thereby providing for consistent element naming within **Claim 10**. No new matter was introduced in amending the claims. Support for the amendments can at least be found in FIGS. 19 through 23B of the **Drawings**, and in Paragraphs 0068 through 0078 of the **Detailed Description**.

Accordingly, as amended herein **Claim 10** provides an antecedent basis for the words "the electrical communication". Therefore, **Claim 10** as amended herein is no longer indefinite and the rejection under second paragraph of **35 U.S.C. §112** ought to now be withdrawn. The rejection of **Claim 11** as depending from rejected base **Claim 10** are mooted by the aforementioned amendments to **Claim 10**. Therefore, the rejection of **Claim 11** under second paragraph of **35 U.S.C. §112** ought to now be withdrawn.

b. Rejection of Claims 10 & 11 under 35 U.S.C. §102(b) (*424 Patent*)

Claim 10 was also amended to recite that the plurality of line driver groups are in electrical communication with a non-volatile two-terminal cross point memory array. Support for the amendment can at least be found in FIGS. 1 through 3B of the **Drawings**, and in Paragraphs 0002 and 0016 – 0021, of the **Detailed Description**. Although "cross point memory array" was previously identified in the preamble, the

element was repeated in the body of the claim to unambiguously indicate the Applicants' intent to incorporate the element in the claim. Without commenting on whether language in the preamble should generally be used to interpret a claim, the scope of **Claim 10** is not intended to be narrowed by the present amendment.

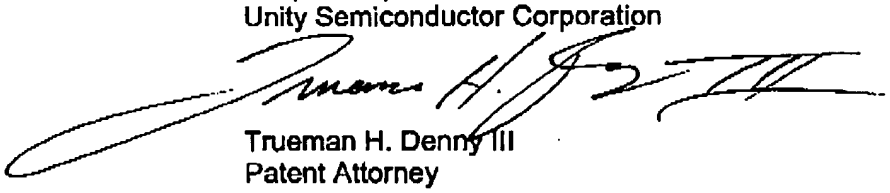
As amended herein, **Claim 10** is not anticipated by *Iwata* because each an every element of **Claim 10** is not explicitly or inherently disclosed in *Iwata* for the following reasons. First, *a non-volatile two-terminal cross point memory array* as recited in **Claim 10** is not identically described in *Iwata* because the MCA: Memory Cell Array of Figs. 7F, 7J, and 7N of *Iwata* is a DRAM memory cell architecture (see cols. 5 & 6 and Fig. 1). It is well understood in the electronics art that DRAM memory is volatile and loses data retention when power is removed from the DRAM. Second, the memory cell in the MCA of *Iwata* is not *a non-volatile two-terminal cross point memory array* because more than two electrically conductive interconnect lines are required to read/write data to a memory cell (i.e. capacitors) in the MCA (see *Iwata* cols. 12 & 13 and Fig. 5). Finally, the DRAM memory cell in the MCA of *Iwata* requires more than two terminals (see *Iwata* Fig. 4), as is well understood in the electronics art.

For the reasons set forth above, all of the elements of **Claim 10** are not explicitly or inherently disclosed in *Iwata*. Therefore, **Claim 10** is patentably distinct and is not anticipated by *Iwata*. Accordingly, the rejection of **Claim 10** under **35 U.S.C. §102(b)** ought to now be withdrawn. Because **Claim 11** depends from **Claim 10** and inherits all of its limitations, **Claim 11** is patentably distinct and is not anticipated by *Iwata*. Therefore, the rejection of **Claim 11** under **35 U.S.C. §102(b)** ought to now be withdrawn.

iii. **Conclusion**

Applicant now believes the present case to be in condition for allowance, and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application the undersigned can be reached at (408) 737-7200 x124.

Respectfully submitted,
Unity Semiconductor Corporation



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